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NAMAN JAIN
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WORK EXPERIENCE

➢ **Bloomberg L.P.**, 731 Lexington Av. New York NY, USA   **June 2015 – Present**
 Software Engineer – Index Apps Team
   • Developed engine to let users build their own rules-based equity indices. These indices can originate from any point-in-time, with support for periodic rebalancing and daily corporate-action adjustments.
   • Initiated usage of *Apache Spark* for end-of-day pricing of thousands of custom created indices.
   • Enhanced support for major fixed-income securities since acquisition of *Bloomberg Barclays Index* business.
   • Heavily worked on app enhancements, Linux migration efforts, MiFid II.
   • Added support to configure default equity-index, useful for various benchmark calculations.
   • Recruiting captain for CMU, involved with FIRST robotics mentoring etc.

EDUCATION

➢ **Carnegie Mellon University**, Pittsburgh, USA   **GPA:** 3.83/4.00   **August 2013 – May 2015**
 Master of Science, Electrical and Computer Engineering

18-640 Computer Architecture	18-648 Real-Time Embedded Systems	15-618 Parallel Computer Architecture
15-745 Optimizing Compilers	18-213 Intro to Computer Systems	
18-765 Digital System Testing	18-743 Energy Aware Computing	

➢ **VIT University**, Vellore, India   **GPA:** 9.03/ 10.00   **July 2009 – May 2013**
 Bachelor of Technology, Electronics and Communication Engineering

SKILLS

Tools: git, gdb, dbx, JIRA, Jenkins, Apache Spark, Splunk   **Platforms:** Linux Variants, Windows, Mac OSX
Languages: C++, C, Java, Javascript   **Scripting:** Python, Shell   **Assembly:** x86, x86-64

ACADEMIC PROJECTS

➢ **Parallel Computer Architecture**, *Carnegie Mellon, Robotics Institute, Spring 2015*
 Implemented a parallel algorithm to localize objects in an image using MPI over multiple machines and cores, and obtained 9x speedup using 32 cores on Intel Xeon E5-2680v2 on AWS. Details at: http://namanjain236.github.io/perception/

➢ **Real-time Embedded Systems**, *Carnegie Mellon, Fall 2014*
   • Implemented 'Resource kernel' framework for real-time tasks by enforcing hard timing constraints on CPU utilization.
   • Implemented multi-processor scheduling using bin-packing heuristics.
   • Introduced a new power-saving governor based on Sys-Clock Algorithm to the kernel.
   • Built an Android application for setting/canceling/monitoring timing reservation on tasks using custom syscalls.

➢ **Energy-Aware Computing**, *Carnegie Mellon, Fall 2014*
   • Simulated heterogeneous architecture using 'big', 'small' cores and determined optimal number of big cores, with respect to number of cores on chip, as 1:4 for most benchmarks.
   • Designed novel IPC-based dynamic scheduling policy.

➢ **Optimizing Compilers**, *Carnegie Mellon, Spring 2014*
 Implemented loop perforation in LLVM compiler to improve performance with bounded accuracy trade-off. Benchmarked simulations proved 1.83x speedup with only ~0.5% accuracy loss in most of the cases.

➢ **Embedded Systems**, *VIT University, 2012-2013*
   • **Humanoid Robot for Industrial Applications:** Built a humanoid robot, *iZac*, capable of walking, climbing and executing highly stabilized hand movements.
   • **Driver Assistance System for Blind Turns:** Designed and implemented the system to avoid accidents on blind turns using automated traffic signals using wireless sensor network.   *Sponsored by DSIR (Govt. of India)*

RESEARCH EXPERIENCE

➢ **Teaching Assistant, Carnegie Mellon University, Pittsburgh**   **May 2014-December 2014**
 Designed course projects for *Computer Architecture* course using gem5 simulator infrastructure.
   • Implemented YAGS and gshare predictor designs. Added instrumentation for instruction buffer and ROB utilization.
   • Implemented replacement policies LRU, LFU and cache coherence protocol (MSI, using SLICC) in gem5.

➢ **Research Intern, Institut Supérieur d'Electronique de Paris (ISEP), Paris**   **Jan 2013-May 2013**
 Resolved limited storage issues of semantic web using sampling operators to drop RDF triples from the incoming data.

ACADEMIC AWARDS & ACHIEVEMENTS

➢ **Indian Patent** (No. 5311/CHE/2012) pending for *Driver Assistance System* project, VIT University, 2012-2013.
➢ **Best Project Runner-up Award**, Poster Presentation, Energy-Aware Computing, Fall 2014.
➢ **NRDC Meritorious Invention Award – 2012**, National Research Development Corporation at Dehradun in 2014.
➢ **1st Prize, IEEE AIYEHUM – 2012** for *Virtually Writing Gloves* at Bangalore in 2012.
➢ **Best Paper Award,** Paper Presentation, **IEEE Eureka** for *Virtually Controlled Robotic Arm* at Kshitij 2012, IIT-K.
➢ Received **Young Achievers Award** at VIT University, Vellore in 2012.